Audial

USB board Mk2

INSTRUCTION MANUAL

Revision 0, December 2017

This manual comprises introducing information on use and performance of this device. For more information please refer to the Audial web site, or send your questions to info@audialonline.com.

IMPORTANT!

1. This manual is a guide only.

2. Device is claimed to work as such, however the customers are responsible for their applications.

3. Do not expose this device to rain or moisture, excessive heat or mechanical force.

4. Use this device exclusively with specified voltages.

5. Unplug the device from the wall outlet during a lighting storm.

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THIS DEVICE

Audial USB board is a USB audio decoding stage, which also generates clock signal for D/A conversion. At one side it connects to PC via USB port and, by operating as asynchronous (master) USB Audio Class 2.0 device, it is able to accept audio sampling rates up to 192 kHz. Up to 384 kHz operation is available as optional feature.

The board decodes USB signal to raw PCM that can be sent to D/A chips. Also, it provides galvanic decoupling between USB and PCM side, thus also separating PC from audio clocks and other audio circuits.

Two low jitter clocks are included, one that works with 44.1/88.2/176.4 kHz, and the other that works with 48/96/192 kHz sampling frequencies. This way the unit achieves clean clocking scheme, and all the audio clock signals in the system are generated only by frequency dividing, and not by using PLL synthesizers.

MARK 2

The Mk2 board version is shipped as a ready made module, or as completed unit.

Modules are intended for use inside or close to the D/A converters, and output signal is available on the set of nine U.FL PCB connectors. These U.FL outputs are 3.3 V level, with 50 Ohm build-out resistors, and they can drive several gates, but are not meant to drive terminated lines. Modules do not include BNC output connectors, nor do they include associated line drivers.

Module requires transformer with two secondary windings: one 7-8 VAC (AC1) for USB front end, and one 8-10 VAC (AC2) for clocking and output side. AC1 can be up to 10 VAC too, but transistor Q1 (BD139, TO-126 package) should have some heatsink in that case.

Transformer should be capable to supply 500mA, for both AC1 and AC2. The current actually needed by AC1 is 100 mA typically (120 mA max). The current needed by AC2 is normally 20-30 mA, but if BNC outputs are added to drive terminated lines, it will increase to about 100 mA. Overall, a small 10 VA transformer is enough to feed this module, and 20 VA is plenty, under any circumstances.

Completed unit includes line output drivers, and PCM signal, including the master clock, is available on the set of BNC connectors, located along the right side of the unit. BNC outputs are typically 5 V level, 75 Ohm series terminated, and with 75 Ohm load they will provide 2.5 V at receiving end, but on request they can be set for 3.3 V output too.

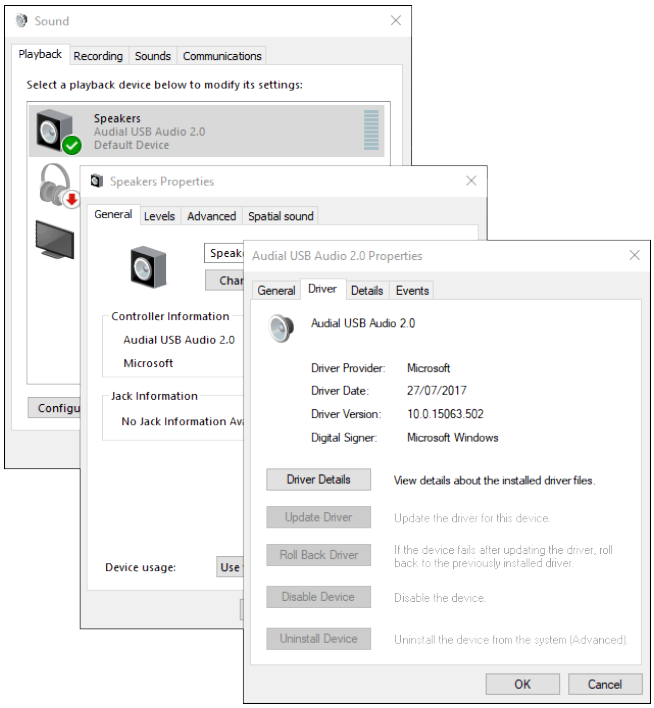
USB AUDIO CLASS 2.0

This USB device employs USB Audio Class 2.0 definitions.

Mac OS X and Linux are natively USB Audio Class 2.0 compliant for several years now, and this device hence does not require special driver when used with Mac OS X or Linux.

WINDOWS USB AUDIO CLASS 2.0

Since September 2017, Windows 10 also supports USB Audio Class 2.0 definitions. This basically makes this device plug and play with Windows 10, and once it is connected to Win 10 machine, the small window will pop up in the bottom right corner of the screen, reporting about the initial connection routine. Once this process is finished, the device can be found as playback audio device, available in the system.

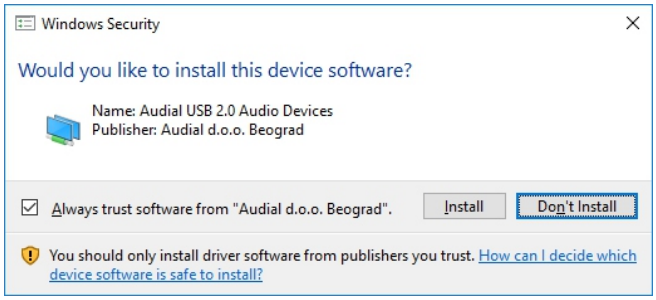


DEDICATED WINDOWS DRIVER

Audial provides dedicated Windows driver for this device, which is still necessary with earlier Windows versions. Also, this driver provides additional functionality as firmware update, ASIO interface, buffer length control, and can be generally preferred soundwise.

Users can download this driver from Audial web site. Driver version 1.26 can be installed to Windows XP, Vista, 7, 8, 8.1 and 10. Later driver version 2.10 however improves on compatibility with later PC systems, and can be installed to Windows 7, 8, 8.1 and 10. All driver versions are compatible with both 32 and 64-bit Windows.

To install the driver, please unzip provided file, and run setup.exe. Installation window will pop up, and at one stage you will be asked to connect the device. Also, during this process, depending on your Windows version and security settings, you might be asked a couple of times to allow the installation, so please do so. These windows will look like this.



Once the installation is complete, you can configure your settings by using the control panel, available in Windows Start Menu -> Audial.

OUTPUT FORMATS

Depending on the firmware, this board may output one of the following digital protocols.

A. Philips simultaneous data protocol

This protocol is intended for use exclusively with TDA1541(A). The output has split channels, 16-bit right justified data, in offset binary format, clocked on the falling edge of BCK. Negative data outputs are also provided, so the board can be used as a source for true balanced TDA1541(A) DAC.

B. I2S/ SPDIF

I2S is as specified, so two data channels are time multiplexed, and binary word starts one BCK cycle after WS transition. Data is in two's complement format, and is clocked on the raising edge of BCK. In addition, the board with I2S output also has an S/PDIF output.

C. PCM1704 format

Similarly to firmware A, this option has split channels, and right justified data. The word is however 24-bit long, data is in two's complement format, and it is clocked on the raising edge of BCK.

Output formats are graphically shown on the figure 4 (page 9).

OUTPUT CONNECTIONS

The table below shows detailed list of the signals available on the set of nine U.FL connectors (J202 - J210). The same applies to the BNC output connectors of the completed unit, and the only exception is that there is only one BNC connector per BCK and LE / WS line.

In I2S mode, 75 Ohm S/PDIF output is available at BNC connector J201, on the back side.

Connector	Output format		
	Simultaneous data	I2S / SPDIF	PCM1704
DL (J202 / J301)	Left channel data	x	Left channel data
DLN (J203 / J302)	Left channel inverted data	x	Left channel inverted data
DRN (J204 / J303)	Right channel inverted data	x	Right channel inverted data
DR / DATA (J205 / J304)	Right channel data	Data	Right channel data
BCK (J206 / J305)	Bit clock	Bit clock	Bit clock
BCK (J207)	Bit clock	Bit clock	Bit clock
LE / WS (J208 / J306)	Latch enable	Word select (a.k.a. LRCK)	Latch enable (WCLK)
LE / WS (J209)	Latch enable	Word select (a.k.a. LRCK)	Latch enable (WCLK)
MCK (J210 / J307)	Master clock	Master clock	Master clock

MAXIMUM SAMPLING RATES

At its input, this device is generally 192 kHz compatible, however maximum output sampling frequency might be limited by the reclocker, and its requirements regarding the master clocks frequencies. Table below shows detailed specifications.

Please note that the TDA1541, both -A and non -A versions, can normally work up to 192 kHz in simultaneous data mode, however in I2S it is limited to 96 kHz in any case.

UP TO 384 KHZ COMPATIBILITY

Firmware version 3.5 has been released in September 2017, to add 352.8 kHz and 384 kHz compatibility to the boards with TDA1541(A) simultaneous data output and 22.5792 / 24.576 MHz master clocks.

Please note that the Windows audio is currently limited to 192 kHz, however the operation at 352.8 kHz and 384 kHz is possible by means of ASIO or WASAPI (exclusive mode) interface.

Also, while non -A version of TDA1541 chip will normally work up to 384 kHz, a TDA1541A will need a small tweak. Please contact us for detailed information.

Master clock frequencies	Firmware	Maximum sampling rate			
		Simultaneous data	I2S	S/PDIF	PCM1704
11.2896 / 12.288 MHz	3v3	192 kHz	96 kHz	96 kHz	192 kHz
22.5792 / 24.576 MHz	3v3	192 kHz	192 kHz	192 kHz	192 kHz
22.5792 / 24.576 MHz	3v5	384 kHz	N/A	N/A	N/A

THIS BOARD AND AYA II 2014 / DS

This board can be easily connected to AYA II DAC projects released in 2014 and 2015 (DS).

Both USB board and AYA II 2014 / DS can operate in both Philips simultaneous data and I2S mode. AYA II 2014 / DS can accept either simultaneous data protocol or I2S at the input connectors J301-J304. At the input connectors J305-J307 it can accept only I2S.

USB board output mode is defined by its firmware. AYA II i.e. TDA1541A mode is set by TDA1541A pin 27, and for simultaneous data mode it should be tied to -5 VDC (pin 26), whereas for I2S it should be tied to +5 VDC (pin 28). This can be done either by PCB DIP switch or by wire jumper. Switch is recommended though, so the mode can be easily changed later.

Preferred mode of operation is simultaneous data mode, for better intrinsic jitter performance of TDA1541(A).

Please however note also that the AYA II can not switch automatically between two modes, so if you settle on simultaneous data mode, you will have to change its mode manually to I2S whenever the other input (S/PDIF or external I2S) is used.

Before connecting this board to AYA II, the connection between AYA II on-board USB stage and its input switching relays must be cut. This can be done by removing (or by pulling up one side of the) resistors R118-R120. This way the U.FL connectors J301-J304 are ready to accept external source.

In addition, is also the good idea to turn AYA II on-board USB stage completely off, by disconnecting its secondary winding AC1.

In simultaneous data mode the connection between two boards is achieved by four U.FL cables (Data L, Data R, BCK, LE), while I2S requires three U.FL cables (Data, BCK, WS).

By making these connections, the whole set-up is ready for operation.

Two boards should be placed one beside the other, into the same plane, and not one above the other.

AYA II 2014 / DS DEM CLOCKING

To determine right DEM clocking frequency, it is important to know what sets its bottom and upper limit. Firstly, a DEM clock frequency is divided by four internally by TDA1541A, and this divided-by-four frequency should never fall into the audio band, because it can produce the glitches of its own. So, practical bottom limit is 80 kHz. On the other side, TDA1541A performance slightly decreases, as DEM frequency increases. While this decrease is in fact not huge, and occurs mostly at the bottom end of the audio spectrum (0.5 dB at 100 Hz, for 400 kHz DEM frequency), it is wise to keep the DEM frequency below 500 kHz.

The AYA II DS on-board DEM clocking circuit takes the bit clock signal, and divides it by 16. This way, in simultaneous data mode (32 bit frame) the DEM frequency will be two times higher than audio sampling frequency, while in I2S (64 bit frame) the DEM frequency will be four times higher than audio sampling frequency. In all these cases, and taking into account the range of operation that applies to each mode, the DEM frequency will always remain between 88.2 kHz and 384 kHz. Therefore, when AYA II DS is used with this module, its DEM clocking circuit can be left as is.

In the AYA II 2014 this synchronous DEM clocking circuit is optional, but users can employ it the same way it is used in the AYA II DS.

Of course, since this module offers also a master clock output, this clock frequency, adequately scaled down, can be also used as a basis for TDA1541A DEM circuit.

LED INDICATORS

The board offers connections for three indicating LE diodes. D10 indicates the board power supply (it is connected to R5-R6/C4, fed by AC2), D101 indicates the USB cable connection (it is connected to USB Vbus), while D102 indicates the audio stream i.e. playback (flag comes from decoding processor).

BOARD SIZE AND MOUNTING

The board size is 110 mm (width) x 120 mm (depth). There are four mounting holes, each 4 mm in diameter, located 5 mm from the board back, left and front edge, and 25 mm from the right edge.

Center of USB connector is 27 mm from left edge of the board. Center of S/PDIF output BNC connector (applies to boards with S/PDIF output) is 67 mm from the left edge of the board.

To determine heights of the holes at the back plate required for these connectors, please consider not only PCB stand-offs, but also PCB itself, which is 1.6 mm thick. The drawing below shows recommended BNC and USB connectors panel cut-out (rear view), taking into account 15 mm stand-offs at that.

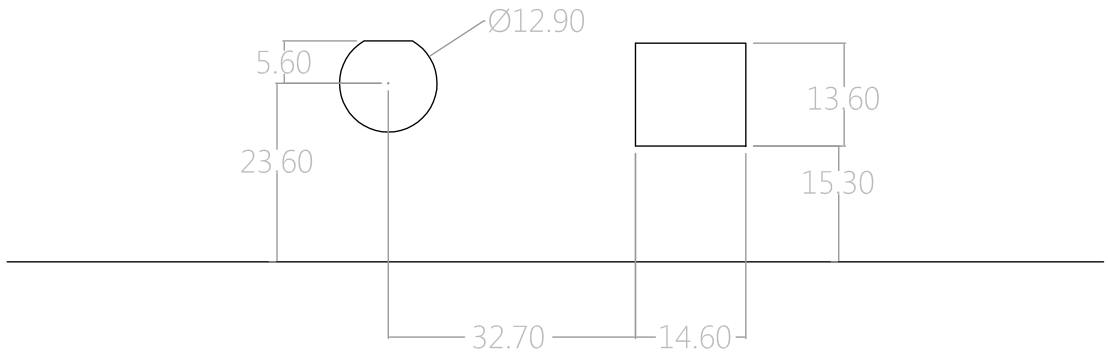


Fig 3: Recommended rear panel cut-out, rear view (all measures in mm)

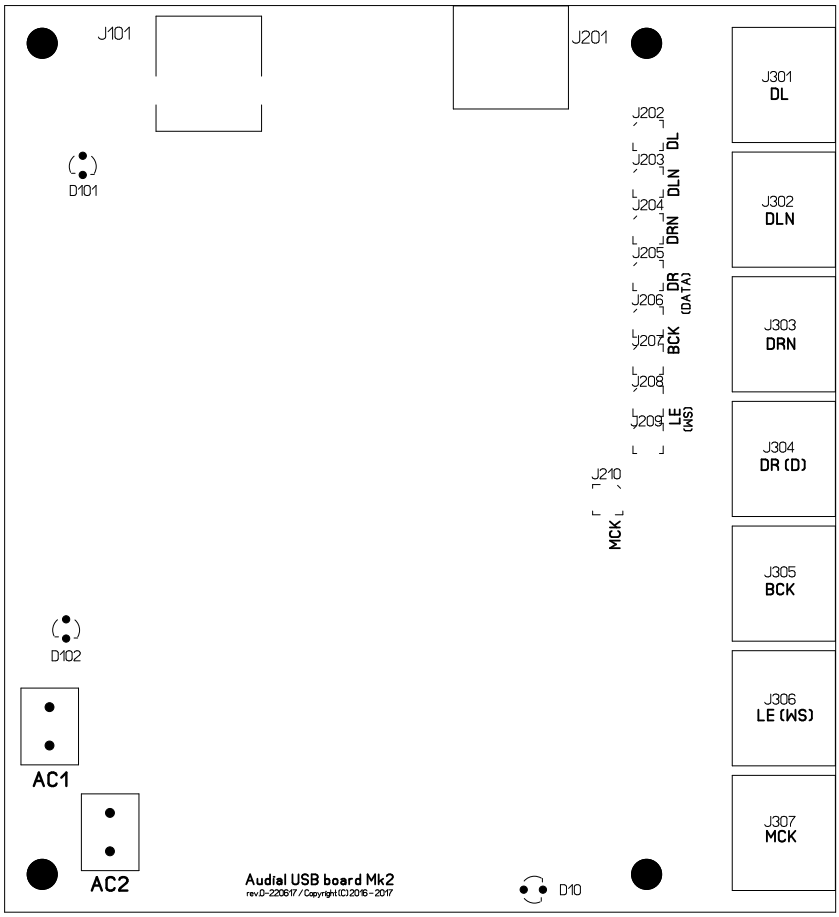


Fig 4: Top side of the board.

The picture shows USB input connector (J101), S/PDIF output connector (J201), U.FL output connectors (J202 - J210), BNC output connectors (J301 - J307) transformer connections (AC1, AC2), LED indicators (D10, D101, D102), and mounting holes

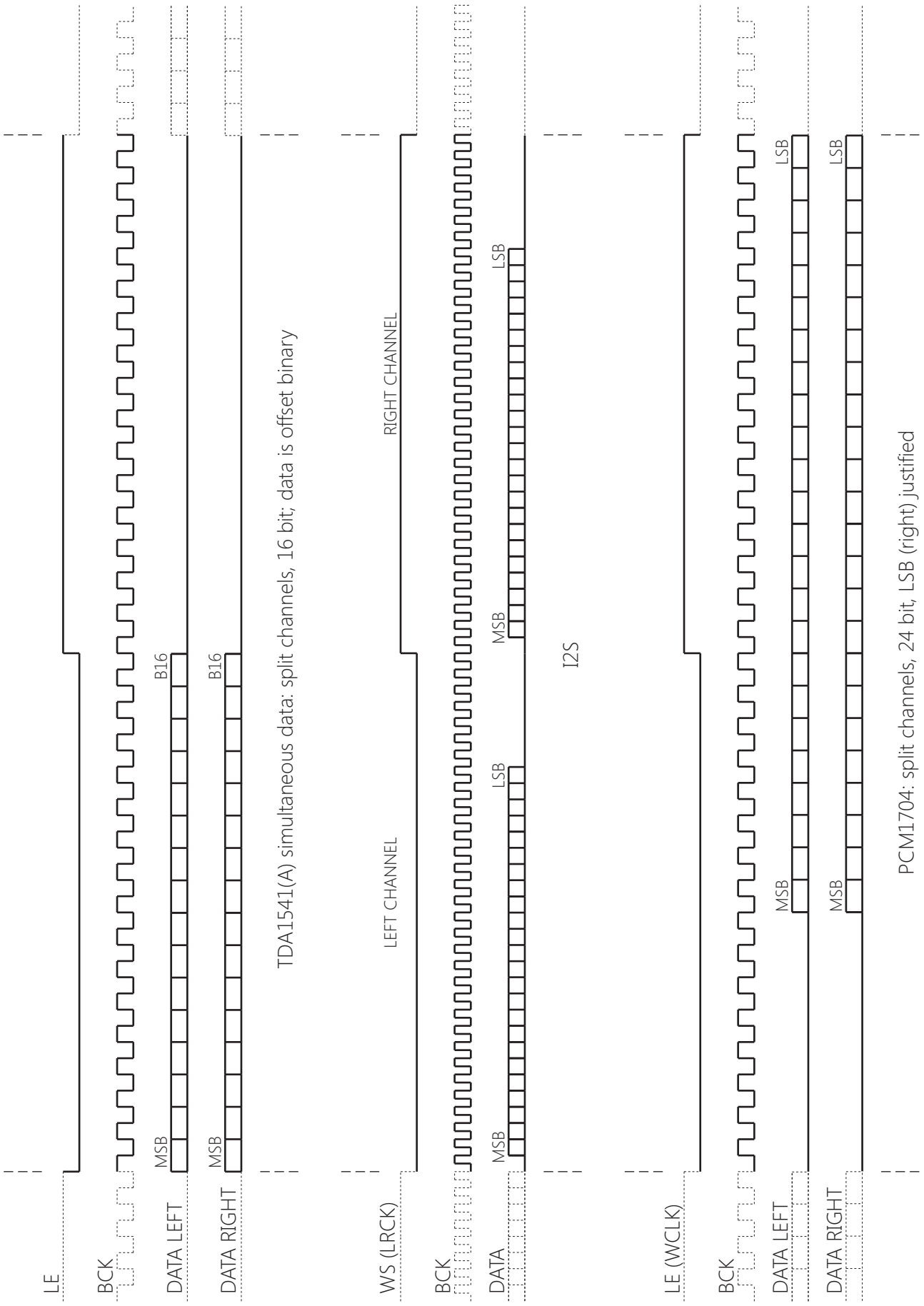


Fig 5: Output formats

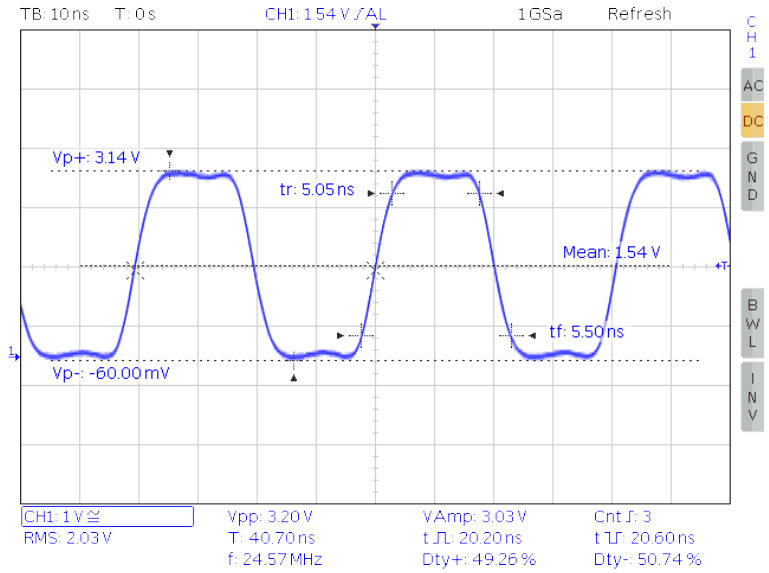


Fig 6: 24.576 MHz master clock, U.FL output, 12 pF load

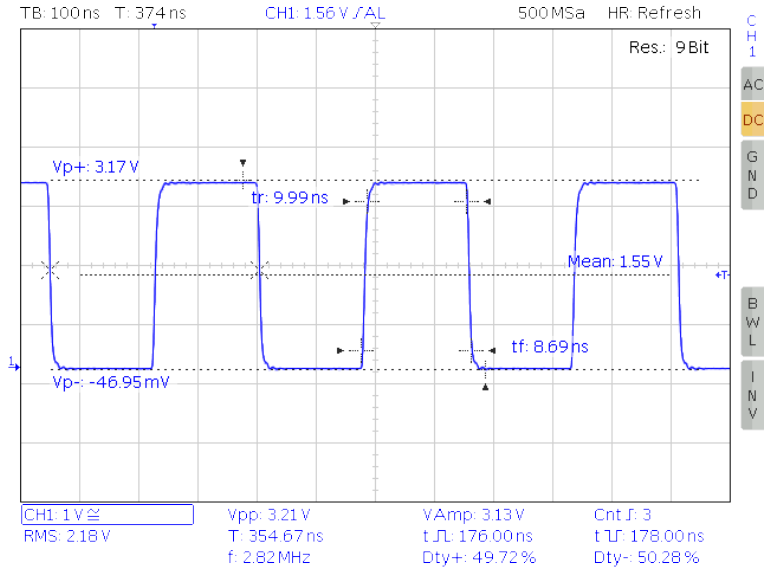


Fig 7: 2.8224 MHz bit clock, U.FL output, 12 pF load

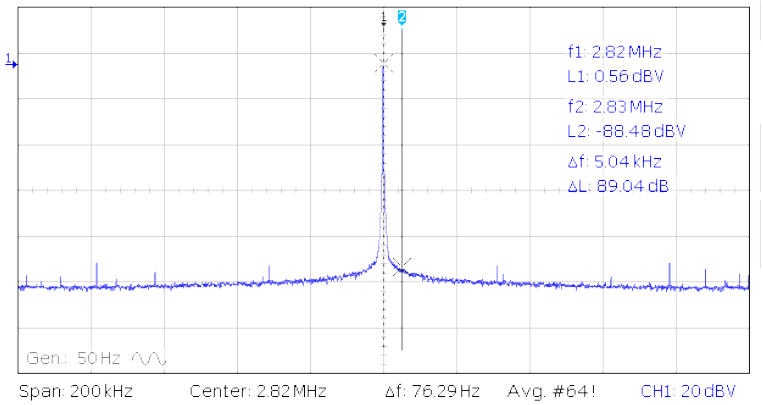


Fig 8: 2.8224 MHz bit clock, U.FL output, spectral analysis, 200 kHz span

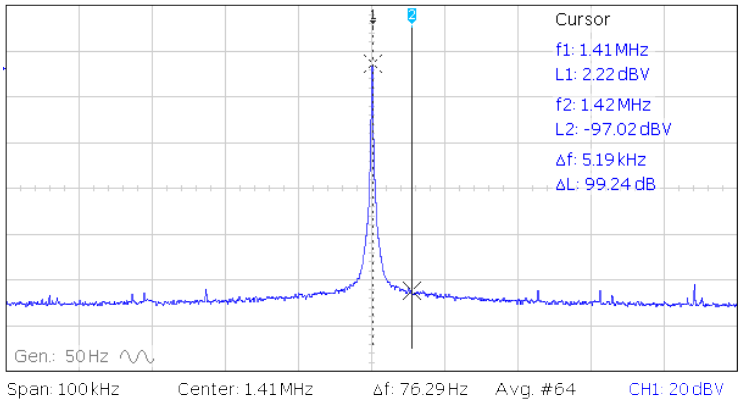


Fig 9: 1.4112 MHz bit clock, U.FL output, spectral analysis, 100 kHz span

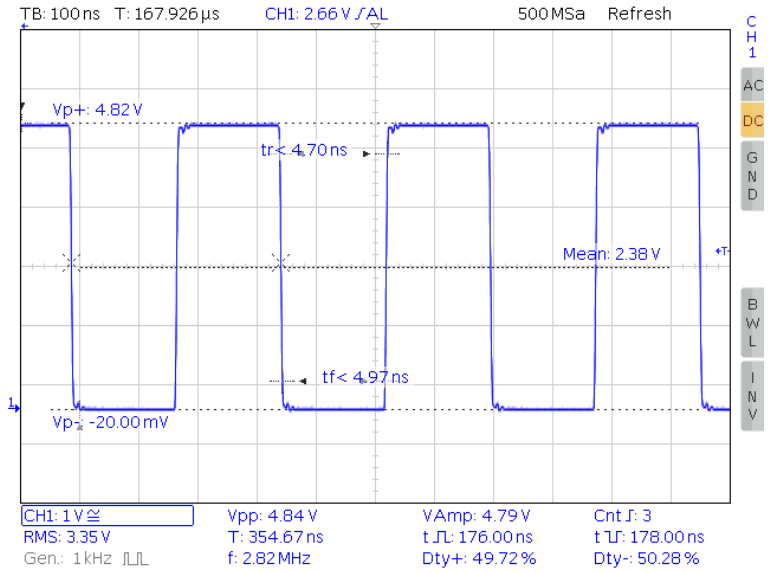


Fig 10: 2.8224 MHz bit clock, BNC output, 12 pF load, no termination

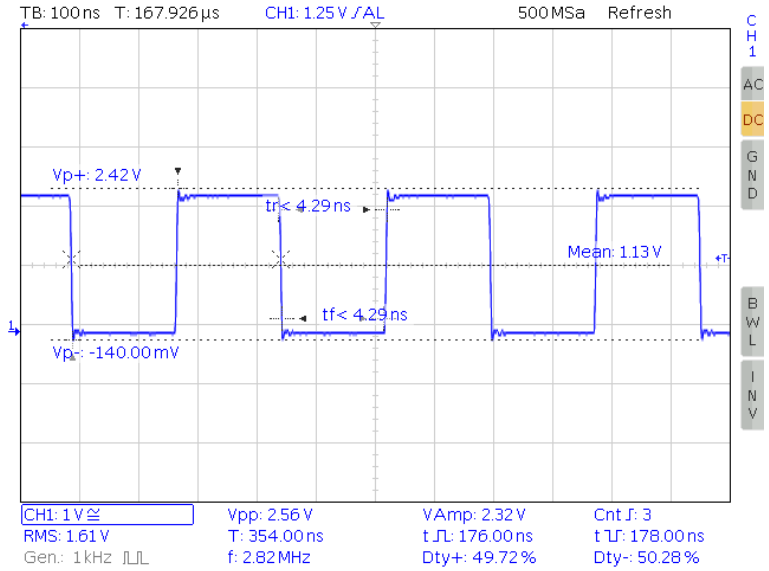


Fig 11: 2.8224 MHz bit clock, BNC output, 75 Ohm ‖ 12 pF load

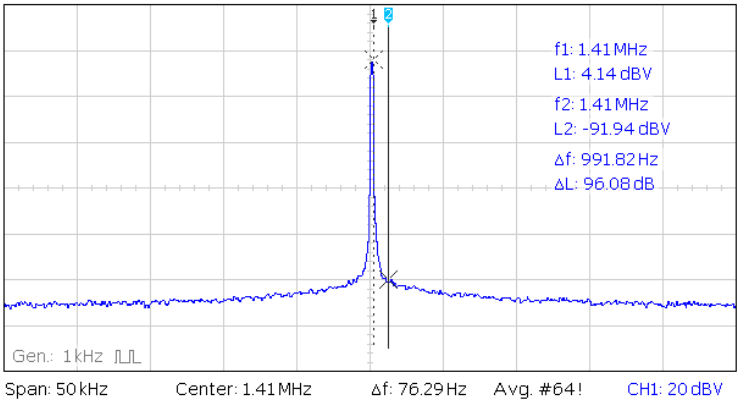


Fig 12: 1.4112 MHz bit clock, BNC output, spectral analysis, 50 kHz span