Audial

USB BOARD

INSTRUCTION MANUAL

Revision A, January 2017

This manual comprises introducing information on use and performance of this device. For more information please refer to the Audial site, or send your questions to info@audialonline.com.

IMPORTANT!

1. This manual is a guide only.

2. Device is claimed to work as such, however the customers are responsible for their applications.

3. Do not expose this device to rain or moisture, excessive heat or mechanical force.

4. Use this device exclusively with specified voltages.

5. Unplug the device from the wall outlet during a lighting storm.

THIS BOARD

Audial USB board is a USB audio decoding stage, which also generates clock signal for D/A conversion. At one side it connects to PC via USB port and, by operating as asynchronous (master) USB Audio Class 2.0 device, it accepts up to 192 kHz sampling rates. On the other side it outputs decoded PCM signal, that can be sent to D/A chips. Also, it provides galvanic decoupling in between.

POWER SUPPLY

This board uses USB +5 VDC (Vbus) to supply USB decoder. On the other, clocking side, it requires one 8-10 VAC transformer secondary winding, to supply clocking circuits, via on-board low noise rectifier and regulator.

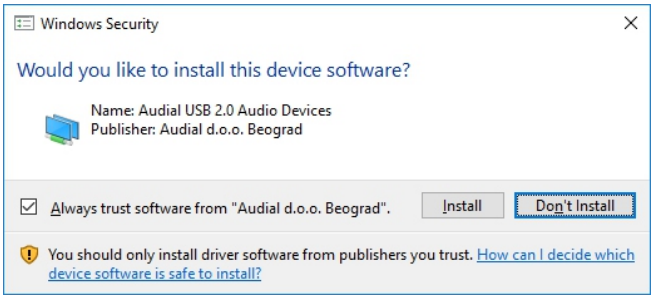
USB AUDIO CLASS 2.0

This board employs USB Audio Class 2.0 definitions. Windows is still not Audio Class 2.0 compliant, and Audial hence provides adequate Windows driver. As opposed to Windows, Mac OS X and Linux support these definitions natively, and do not require special driver.

WINDOWS DRIVER

Audial USB board users can download Windows driver from Audial web site. It can be installed to Windows XP, Vista, 7, 8, 8.1 and 10.

To install the driver, please unzip provided file, and run setup.exe. Installation window will pop up, and at one stage you will be asked to connect the device. Also, during this process, depending on your Windows version and security settings, you might be asked a couple of times to allow the installation, so please do so. These windows will look like this.



Once the installation is complete, you can configure the settings by using the control panel, available in Windows Start Menu -> Audial.

OUTPUT FORMATS

Depending on the firmware, the board may output one of the following digital protocols.

A. Philips simultaneous data protocol

This protocol is intended for use exclusively with TDA1541(A). The output has split channels, 16-bit right justified data, in offset binary format, clocked on the falling edge of BCK. Negative data outputs are also provided, so the board can be used as a source for true balanced TDA1541(A) DAC.

B. I2S/ SPDIF

I2S is as specified, so two data channels are time multiplexed, and binary word starts one BCK cycle after WS transition. Data is in two's complement format, and is clocked on the raising edge of BCK. In addition, the board with I2S output also has an S/PDIF output.

C. PCM1704 format

Similarly to firmware A, this option has split channels, and right justified data. The word is however 24-bit long, data is in two's complement format, and it is clocked on the raising edge of BCK.

Output formats are graphically shown on the figure 4 (page 9).

MASTER CLOCKS

The board employs low jitter clocks made by AVX. There are two clocks, one that works with 44.1/88.2/176.4 kHz, and the other that works with 48/96/192 kHz sampling frequencies. This way the board achieves clean clocking scheme, and generates all the other clock signals in the system only by frequency dividing, and not by using PLL synthesizers.

The board may have one of two possible clock pairs: 11.2896 MHz / 12.288 MHz, or 22.5792 MHz / 24.576 MHz. The first pair provides proper work for all the PCM output protocols, so simultaneous data, I2S and PCM1704 protocol, however S/PDIF output in that case can not output 176.4 kHz and 192 kHz. To ensure proper work of S/PDIF output up to 192 kHz, a 22.5792 MHz / 24.576 MHz master frequencies are necesary.

FIRMWARE

Firmware is stored in flash memory chip (Q108). Each board or memory chip is marked with letter (A, B or C) and number (1 or 2), that denote the output protocol and master clock frequencies.

	Master clock frequencies (MHz)	
Output	11.2896 / 12.288	22.5792 / 24.576
Simultaneous data	A1	A2
I2S / SPDIF	B1	B2
24-bit PCM1704	C1	C2

OUTPUT CONNECTIONS

The output signals are available at the set of nine U.FL connectors (J202 - J210), located along the right edge of the board.

The signals for each particular format are given in table below.

Electrically, the output is 3.3 V, with 50 Ohm build-out series resistor. It can drive usual U.FL cables and several gates, but it is not meant to drive terminated lines.

In I2S mode, 75 Ohm S/PDIF output is available at BNC connector J201.

Connector	Output format		
	Simultaneous data	I2S / SPDIF	PCM1704
J202 (DL)	Left channel data	x	Left channel data
J203 (DLN)	Left channel inverted data	x	Left channel inverted data
J204 (DRN)	Right channel inverted data	x	Right channel inverted data
J205 (DR / DATA)	Right channel data	Data	Right channel data
J206 (BCK)	Bit clock	Bit clock	Bit clock
J207 (BCK)	Bit clock	Bit clock	Bit clock
J208 (LE / WS)	Latch enable	Word select (a.k.a. LRCK)	Latch enable (WCLK)
J209 (LE / WS)	Latch enable	Word select (a.k.a. LRCK)	Latch enable (WCLK)
J210 (MCK)	Master clock	Master clock	Master clock

MAXIMUM SAMPLING RATES

Generally, the board is 192 kHz compatible, but there are some exceptions in actual use. The table below shows detailed specifications.

Please also note that the TDA1541A can work up to 192 kHz in simultaneous data mode, but it will be limited to 96 kHz in I2S in any case, due to 64 bit length of I2S frame, and 6.4 MHz limit of TDA1541A BCK pin.

Master clock frequencies	Maximum sampling rate at output			
	Simultaneous data	I2S	SPDIF	PCM1704
11.2896 / 12.288 MHz	192 kHz	96 kHz	96 kHz	192 kHz
22.5792 / 24.576 MHz	192 kHz	192 kHz	192 kHz	192 kHz

THIS BOARD AND AYA II 2014 / DS

This board can be easily connected to AYA II DAC projects released in 2014 and 2015 (DS).

Both USB board and AYA II 2014 / DS can operate in both Philips simultaneous data and I2S mode. AYA II 2014 / DS can accept either simultaneous data protocol or I2S at the input connectors J301-J304. At the input connectors J305-J307 it can accept only I2S.

USB board output mode is set by its firmware. AYA II i.e. TDA1541A mode is set by TDA1541A pin 27, and for simultaneous data mode it should be tied to -5 VDC (pin 26), whereas for I2S it should be tied to +5 VDC (pin 28). This can be done either by PCB DIP switch or by wire jumper. Switch is recommended though, so the mode can be easily changed later.

Preferred mode of operation is simultaneous data mode, for better intrinsic jitter performance of TDA1541(A).

Please however note also that the AYA II can not switch automatically between two modes, so if you settle on simultaneous data mode, you will have to change its mode manually to I2S whenever the other input (S/PDIF or external I2S) is used.

Before connecting this USB board to AYA II, the connection between AYA II on-board USB stage and its input switching relays must be cut. This can be done by removing (or by pulling up one side of the) resistors R118-R120. This way the U.FL connectors J301-J304 are ready to accept external source.

It is also the good idea to turn AYA II on-board USB stage completely unpowered, by disconnecting AC1 secondary winding from AYA II board, and to use the same winding to supply this USB board instead. This is also probably the simplest way to use this board: apart from the board itself, a set of U.FL cables is all that is necessary.

In simultaneous data mode the connection between two boards is achieved by four U.FL cables (Data L, Data R, BCK, LE), while I2S requires three U.FL cables (Data, BCK, WS).

By making these connections, the whole set-up is ready for operation.

Two boards should be placed one beside the other, into the same plane, and not one above the other.

AYA II 2014 / DS DEM CLOCKING

To determine right DEM clocking frequency, it is important to know what sets its bottom and upper limit. Firstly, DEM frequency is divided by four internally by TDA1541A, and this divided-by-four frequency should never fall into the audio band, because it can produce the glitches of its own. So, practical bottom limit is 80 kHz. On the other side, TDA1541A performance slightly decreases, as DEM frequency increases. While this decrease is in fact not huge, and occurs mostly at the bottom end of the audio spectrum (0.5 dB at 100 Hz, for 400 kHz DEM frequency), it is wise to keep the DEM frequency below 500 kHz.

Therefore, when used with this USB board, the AYA II DS on-board DEM clocking circuit, which takes the bit clock signal and divides it by 16, can be left as is. This way, in simultaneous data mode (32 bit frame) the DEM frequency will be two times higher than audio sampling frequency, while in I2S (64 bit frame) the DEM frequency will be four times higher than audio sampling frequency. In all these cases, and taking into account the range of operation that applies to each mode, the DEM frequency will remain between 88.2 kHz and 384 kHz.

In the AYA II 2014 this synchronous DEM clocking circuit is optional, but users can employ it the same way it is used in the AYA II DS.

Of course, since this USB board offers also a master clock output, this clock frequency, adequately scaled down, can be also used as a basis for TDA1541A DEM circuit.

LED INDICATORS

The board offers connections for three indicating LE diodes. D1 indicates the power for clocking circuits (AC1), D101 indicates the USB stage power, i.e. voltage available at USB line, while D102 indicates the audio stream.

BOARD SIZE AND MOUNTING

The board size is 95 (width) x 105 (depth) mm. Centers of mounting holes are located 5 mm from board edges, and holes diameters are 4 mm.

Center of USB connector is 27 mm from left edge of the board. Center of S/PDIF output BNC connector (applies to boards with S/PDIF output) is 67 mm from the left edge of the board.

To determine heights of the holes at the back plate required for these connectors, please consider not only PCB stand-offs, but also PCB itself, which is 1.6 mm thick. The drawing below shows recommended BNC and USB connectors panel cut-out (rear view), taking into account 15 mm stand-offs at that.

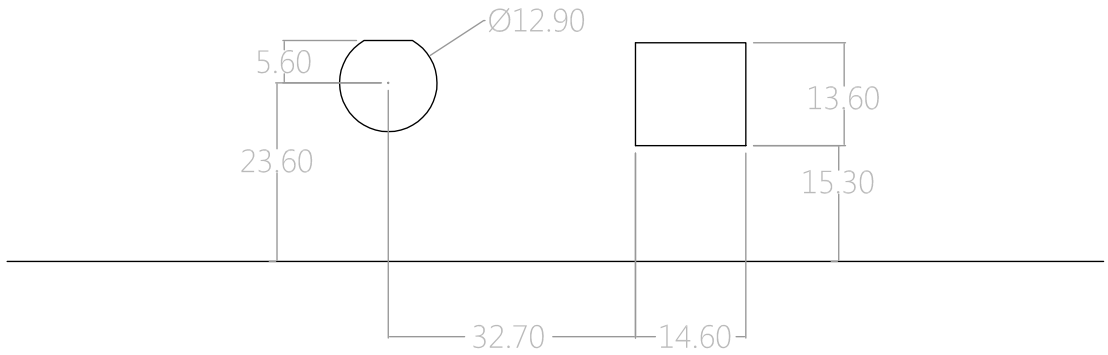


Fig 2: Recommended rear panel cut-out (all measures in mm)

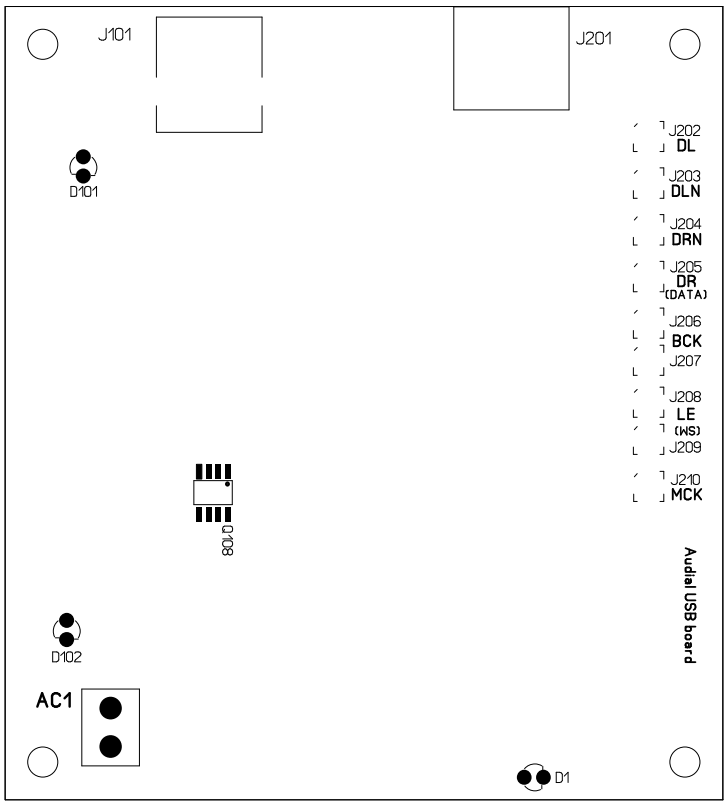


Fig 3: Top side of the board.

The picture shows USB input connector (J101), U.FL output connectors (J202 - J210),
S/PDIF output connector (J201), transformer connection (AC1),
LED indicators (D1, D101, D102), and flash memory chip (Q108)

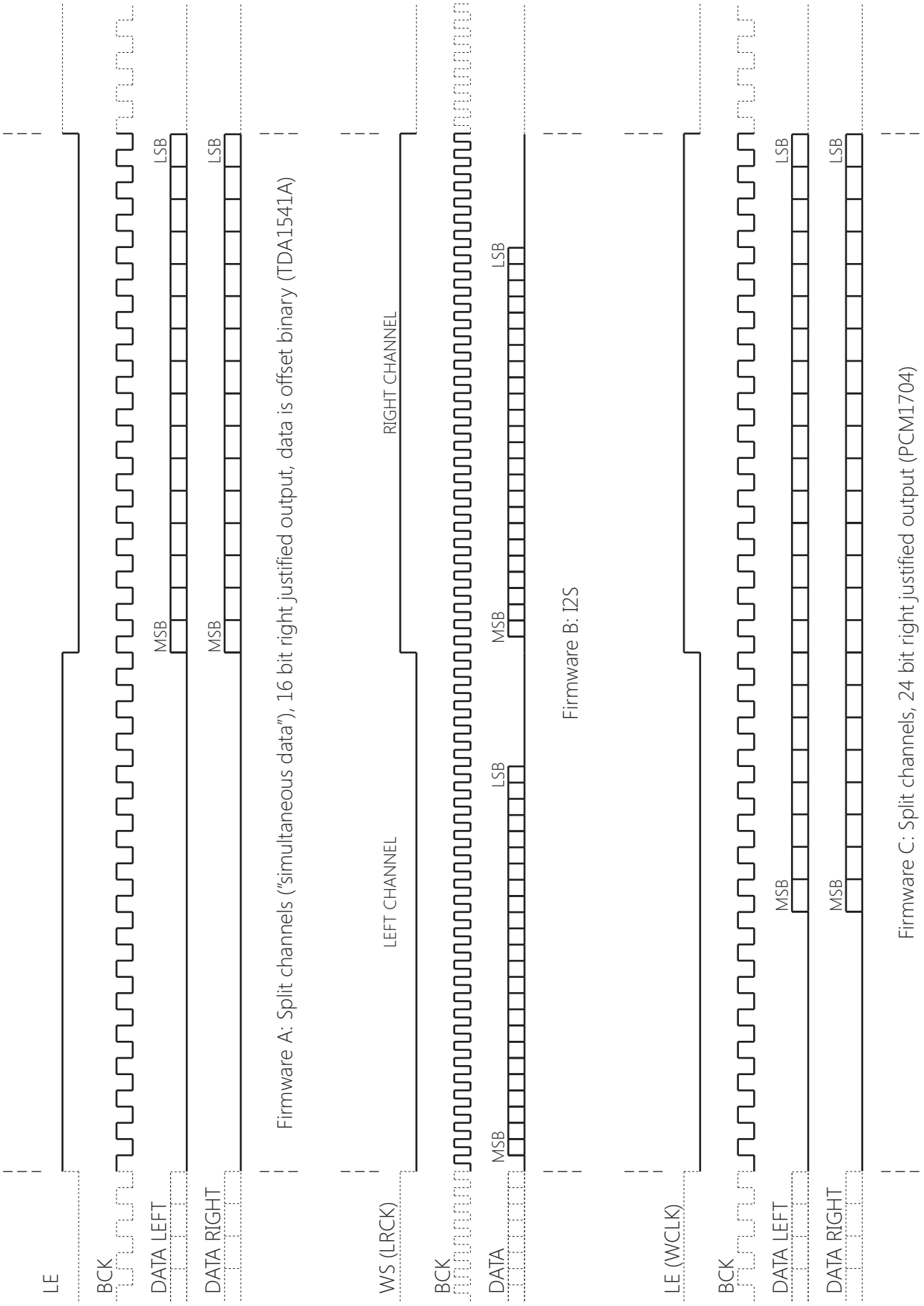


Fig 4: Output formats

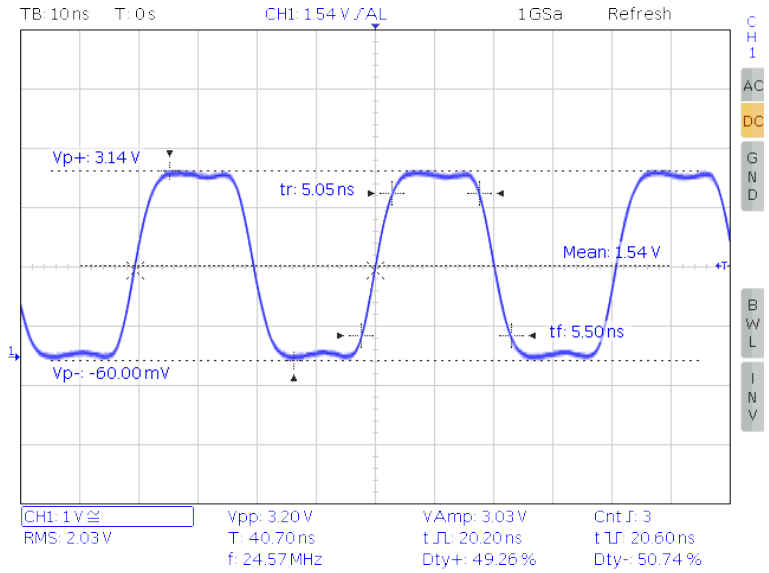


Fig 5: 24.576 MHz master clock output

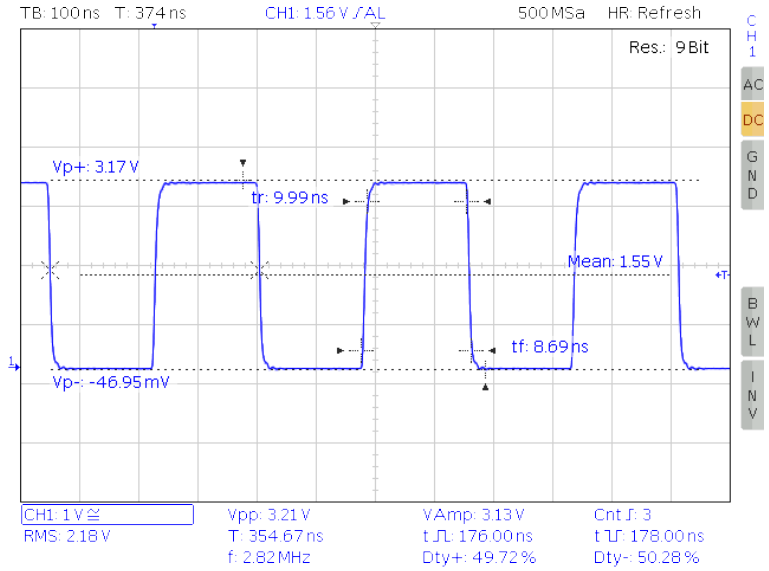


Fig 6: 2.8224 MHz bit clock output

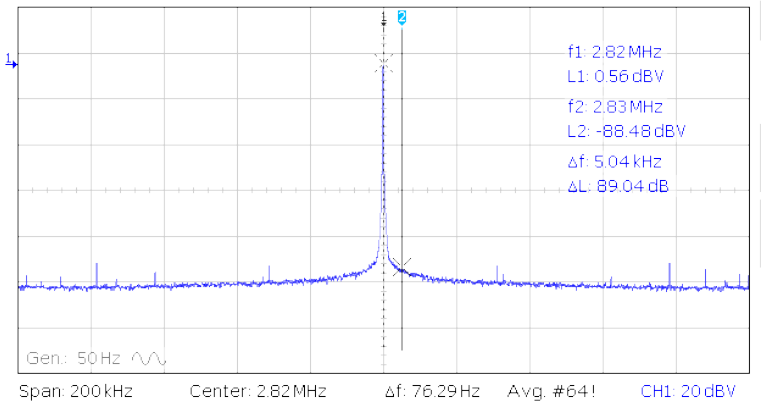


Fig 7: 2.8224 MHz bit clock spectral analysis (200 kHz span)

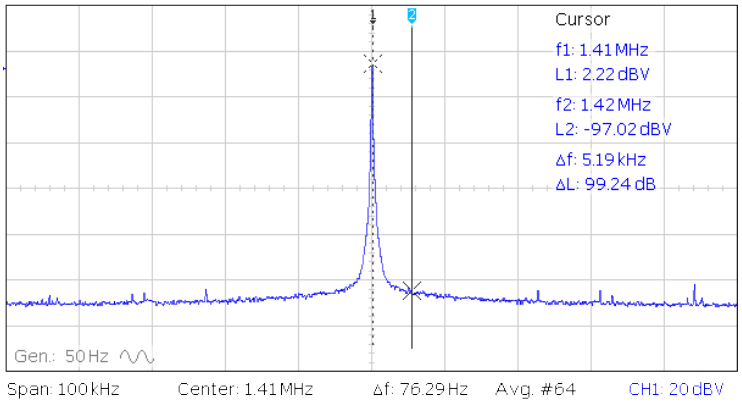


Fig 8: 1.4112 MHz bit clock spectral analysis (100 kHz span)